

Date

 Deadline
CONTACT

Organisation	University of Applied Sciences Northwestern Switzerland	Department	Institute of Microelectronics
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Country	Switzerland		

 Are you familiar with the European Framework Programme? YES NO

TOPIC OF WP¹
Title: Space Technologies
 ASICs for space applications

Number: SPA.2010.2.2-01

Project type	<input checked="" type="checkbox"/> Large-scale integrating collaborative project	<input checked="" type="checkbox"/> Small or medium-scale focused research collaborat. project	<input checked="" type="checkbox"/> Targeted to SMEs	<input type="checkbox"/> Other (Marie Curie Actions, ERA-NET...)
	<input type="checkbox"/> Coordination and Support Action	<input type="checkbox"/> Network of Excellence	<input type="checkbox"/> Research for the benefit of SMEs	
Call references	<input checked="" type="checkbox"/> 3 rd call SPACE			

Intended contribution to research topic :

- Development of very high speed (1–10 Gbit/s) links and networks for components/units interconnections.
- Development and validation of high speed European ADC/DAC
- Development of radiation hard, long life-time libraries for commercial DSM, definition of "platform ASIC architecture" ASIC technology including High Speed Serial Link (as hard macro and standalone chip).

Expertise of the partner

- Design of clock/data recovery for high-speed serial link (40 Gbit/s) in deep sub-micron CMOS technologies (90 nm).
- Design and layout of circuits realized in deep submicron CMOS (≤65 nm)
- Design of flash, ramp and successive approximations ADC and DAC
- Development of rad-hard library elements for a 250 nm CMOS technology
- Field simulations for RF applications
- Synchronisation of multiple serial data streams (skew compensation)
- Rapid prototyping using FPGAs
- Design and analysis of communications channels
- Coding, encryption, decryption, equalization, pre-distortion, synchronization

¹ For details and description of research topics, please visit <http://cordis.europa.eu/fp7/>

key competences (beyond state of the art)	<ul style="list-style-type: none"> • design of CMOS and InP ASIC circuits running at frequencies of 40 GHz+ • design of SIGMA/DELTA converters and systems • design of analogue and digital filters incl. adaptive filters
references /patents	<ul style="list-style-type: none"> • "A 5.75 to 44 Gb/s Quarter Rate CDR With Data Rate Selection in 90 nm Bulk CMOS", IEEE Journal of Solid-State Circuits, Vol. 44, No. 7, pp. 1927–1941, Jul. 2009 and European Solid-State Circuits Conference, 15.–19. Sep. 2008, Edinburgh • "A 300 Hz 19b DR Capacitive Accelerometer Based on a Versatile Front End in a 5th-Order Delta Sigma Loop", to be presented at European Solid-State Circuits Conference, 14.–18. Sep. 2009, Athens
Keywords²	ASIC, high-speed, serial interface, deep submicron, FPGA
Partners to be involved	

Profile of SME / partner sought

Role	<input checked="" type="checkbox"/> technology development	<input type="checkbox"/> research	<input type="checkbox"/> training
	<input type="checkbox"/> dissemination	<input type="checkbox"/> demonstration	<input type="checkbox"/> other _____
Country /region			
Complementary expertise identified or suggested	<ul style="list-style-type: none"> • System integration • CMOS technology provider 		

I agree with the publication of my contact data: YES NO

PLEASE FILL IN THE PARTNER SEARCH FORM AND RETURN IT TO:

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² In accordance with the work program